II. Rejections

With regard to the Office Action, Claims 1 and 3 are rejected as anticipated by U.S. Patent No. 5,495,570 to Huegel by itself. Further, the Office Action alleges that Claims 1 and 3 are obvious in light of the combination of the '570 Huegel patent and U.S. Patent No. 5,590,349 to Robinson et al., and that Claims 2, 4, and 5 are obvious in light of the '570 Huegel patent and the '570 Robinson patent further in combination with Japanese Patent No. 61-3450 to Hirose. Applicant respectfully disagrees with these rejections for the reasons discussed below.

III. The Claims Are Not Anticipated

Applicant submits that the '570 Huegel patent does not teach or suggest concurrent access of data stored in a memory, as is recited in independent Claim 1. Specifically, in this regard, the Office Action alleges that the '570 Huegel patent "may be seen as teaching that the multiple port memories provide internally concurrent access, since the recited memory may be considered to include the interfaces and since the copying via DMA by an out-of-service processor may access the memory while the in-service-processor continues normal operation." (emphasis added). Applicant wishes to draw attention to the last part of the phrase recited by the Office Action. Specifically, the term concurrent as used in the '570 Huegel patent does not mean concurrent access of memory. Instead, it means that one processor can continue to operate, while another processor accesses its memory and not that both processor can access the same memory concurrently.

The specification of the '570 Huegel patent clearly discloses that the system does not allow both processors to concurrently access data stored in a memory via a port. For example, at col. 5, lines 28-36, the specification of the '570 Huegel patent states:

> The present mirrored memory design facilitates concurrent and independent execution of both microprocessors of a pair. This form of concurrent execution is constrained only when both MPU's are attempting memory accesses involving the remote MPU's RAM unit, when both MPU's are competing for a single interprocessor bus (due to failure of one of the two interprocessor busses), or when both MPU's attempt a simultaneous READ-MODIFY-WRITE memory access cycle.

(emphasis added). Further, at col. 6, lines 22-36, the specification of the '570 Huegel patent states:

> Therefore, the invention provides that both MPU's 24, 24' of a pair of processor units share mirrored memory areas in the RAM units 20, 20' in the most literal sense, and co-exist with complete parity with respect to their right to allocate and access both "local" memory and "remote" memory. However, as with any pool of allocatable memory, concurrent access contention (either intraprocessor or interprocessor) requires that memory allocations be coordinated with a locking mechanism. In the present invention, access contention is resolved on a first-come, first-serve basis, in known fashion. Each MPU locks the entire memory area that it accesses during a WRITE operation. MPU's have the right to allocate mirrored memory as they choose, so long as the allocation action yields to prior resource locks on the mirrored memory.

(emphasis added).

As illustrated in these two passages, the system of the '570 Huegel patent does not allow two processors to concurrently access the same memory. Specifically, as stated, a first processor can only access a second processor's memory, when the second processor is not accessing its own memory. If both processors are attempting to access the same memory, then a locking mechanism is implemented so as to allow only one of the processors access. Thus, it respectfully submitted that the '570 Huegel patent does not anticipate independent Claim 1, as it fails to teach or suggest concurrent access of data stored in a memory, as is recited in independent Claim 1.

IV. The Claims Are Non-Obvious

Applicant further submits that independent Claim 1 is not obvious in light of the combination of the '570 Huegel patent with the '349 Robinson patent. Specifically, as discussed above, the '570 Huegel patent nowhere teaches or suggests providing concurrent access to a memory. In fact, it specifically states that concurrent access is not possible in the disclosed circuit. The '349 Robinson patent briefly mentions that the memory may be configured as a true multiport memory, but that is all that is said. It does not disclose how such circuit would operate in a concurrent access manner or teach or suggest to one of ordinary skill in the art as to how the disclosed circuit could be reconfigured to provide concurrent access. Despite what is stated in the Office Action, the '349 Robinson patent nowhere teaches or suggests the advantages of

providing concurrent access. In fact, the '349 Robinson patent states that it is preferable to configure the disclosed circuit in a time division multiplexing format that allows only one processor at a time to access the memory, as opposed to configuring the circuit to allow concurrent access. See '349 Robinson patent, col. 8, lines 25-31.

Applicant respectfully submits that it would not have been obvious at the time of the invention to combine the '570 Huegel patent and the '349 Robinson patent. The '570 Huegel patent clearly discloses a circuit that does not allow concurrent memory access and actually uses a locking mechanism to stop such access. Further, the '349 Robinson merely mentions a true multiport memory configuration, but does not disclose how such a configuration would be constructed or operated. The '349 Robinson also does not list it as a preferred embodiment, much less discuss the advantages of such a circuit. Therefore, Applicant can find no teaching or suggestion in either reference that would lead one skilled in the art to combine the references. Without such a teaching or suggestion, combining these references is impermissible.

Furthermore, Applicant is not sure how such a combined circuit would work. The '570 Huegel patent clearly states that it does not allow concurrent access by using a locking mechanism. Further, the '349 Robinson patent includes no disclosure on how to operate the circuit in a concurrent memory access manner. It is thus, Applicant's conclusion that such a combined circuit would not provide "a plurality of multi-port memories, wherein each memory has at least two ports, wherein each port has a concurrent-access function that allows for internally concurrent access via the port to data stored in the memory," as is recited in independent Claim 1. As such, Applicant respectfully submits that independent Claim 1, as well as the claims that depend therefrom, is patentable over the cited references.

CONCLUSION

In view of the remarks presented above, it is respectfully submitted that all of the present claims of the application are in condition for immediate allowance. It is therefore respectfully requested that a Notice of Allowance be issued. The Examiner is encouraged to contact Applicant's undersigned attorney to resolve any remaining issues in order to expedite examination of the present application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 4, 2004

W. Kevin Ransom